Q.P. Code: 16CS524 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year II Semester Supplementary Examinations March-2021

COMPILER DESIGN

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1 **a** How many phases are there in a compiler? Explain each phase in detail? **[8M]**

b What is Bootstrapping? Write a short note on Bootstrapping. **[4M]**

OR

2 **a** Explain Language Processing system in compiler Design? **[8M]**

b Explain Input Buffering with simple examples? **[4M]**

UNIT-II

3 **a** Construct the recursive decent parser for the following grammar? **[6M]**

E-> E+T/T T-> T*F/F F-> (E)/id

b Explain about Left factoring and Left Recursion with an example? **[6M]**

OR

4 Consider the grammar **[12M]**

S->AB|ABad A->d E ->b D->b| ε B->c

Construct the predictive parsing table. Show that the given grammar is LL(1) or not

UNIT-III

5 **a** Define L attribute and S attribute? Write the differences between L attribute and S attribute with suitable examples. **[6M]**

b Explain the Type Checking with suitable examples? **[6M]**

OR

6 **a** List and Explain different types of intermediate code representations with suitable examples. **[12M]**

UNIT-IV

7 What is Data flow analysis? Explain about Global data flow analysis with example. **[12M]**

OR

8 Explain Storage allocation strategies with suitable examples? **[12M]**

UNIT-V

9 **a** Define what is peephole optimization? Write the role of peephole optimization in compilation process. **[7M]**

b Explain the applications of DAG. **[5M]**

OR

10 Write short notes on **[12M]**

i)Simple code generator

ii) Register allocation

*** END ***